



Effects of Via Slots, Split Planes, Gaps and Return Paths on Clock Signals

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Introduction

The purpose of this experiment was to illustrate some of the basic design techniques regarding clock traces with respect to slots that are created by adjacent vias, split planes, gaps in planes and return paths. It is a commonly taught practice to minimize loop area (that is, to keep the return path for high speed and other critical signals as short as possible). I wanted to look at some of the situations that the PCB design engineer may face when laying out a board, and what actually happens in real life if a designer must compromise good design techniques because of some other physical constraint. I primarily wanted to see how each of these design compromises affects overall EMI emissions. I will also suggest ways in which these undesirable situations can be altered to possibly improve results.

Explanation of example PCB

The PCB designed for this experiment consists of six individual sections, labeled TRACE No. 1 – TRACE No. 6 (Figure No. 1

below shows the bottom side of the PCB). Each section consists of a 50MHz oscillator driving a trace. There are also pads for three passive components, but they are not used except for a 0 ohm resistor in the location for a series resistor in the clock line (these pads were included for future experimentation). In each section, other than the first, I have illustrated an example of a situation to avoid if possible. The PCB constructed was a two layer 0.062” thick board. The signal traces and power distribution are on the top layer, and the bottom layer consists of individual copper fills that act as ground planes (TRACES 1 – 4). On Traces 5 and 6, the return path is a trace on the bottom side.

The power and ground for each section can be completely isolated from the other sections by removing jumpers. This was done so that when I was making measurements on a specific trace, the results would not be influenced by the other oscillators coupling back through the power and ground.

Explanation of each trace and findings

TRACE No. 1 – Trace No. 1 is an example of an ideal situation. The ground plane under the trace is complete for the entire length of the trace, from the output of the oscillator to the output connector. In this situation, we expect that the trace will maintain a constant impedance for the entire length of the trace.

Figure No. 2 is a plot from a network analyzer showing trace impedance versus distance. Marker No. 1 points out a large impedance mis-match due to the output BNC connector. Marker No. 2 shows a slight mis-match due to the series 0 ohm resistor, and marker No. 3 shows a slight mis-match due to the output of the 50MHz oscillator. The point to note from figure No. 2 is that the trace maintains relatively constant impedance from the 0 ohm

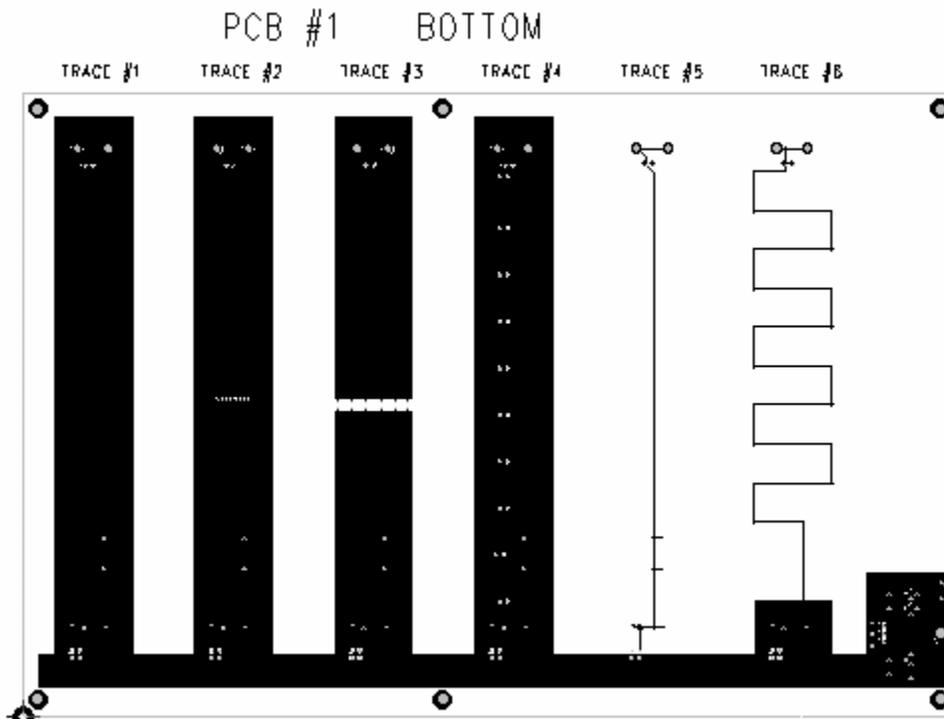


Figure No. 1

resistor to the output connector.

TRACE No. 2 - Trace No. 2 is an example of a trace that is running over a slot in the ground plane. This slot was created by adjacent vias that did not have sufficient clearance to allow the copper fill to penetrate and connect between the vias. One would expect to have a slight impedance mis-match where the trace goes over the slot. The slot in effect forces the return current to take a slightly longer path than the return currents in Trace No. 1.

TRACE No. 3 – Trace No. 3 is an example of a trace that goes over a gap between adjacent planes. This situation could occur in a design that has multiple voltage planes on a single power layer, or where there is a need to have different ground planes on a single layer (possibly analog and digital grounds). This is a more drastic example of a slot – basically a slot that is infinitely long.

Figure No. 3 shows the impedance versus distance plot for Trace No. 3. The plot illustrates the same impedance mis-matches as figure No. 2, but with one significant addition. Note the mis-match shown by marker No. 1 in figure No.3 – this is the impedance mis-match caused by the clock trace crossing the gap in the ground plane. (The plot for Trace No. 2 had a similar mis-match due to the slot, but it was not as drastic.)

(TRACES No. 4 – 6 were on the board for future experimentation.)

Conclusion

The situation shown with TRACE No. 2 and TRACE No. 3 occurs frequently. I typically encounter this situation when I'm concentrating on getting the critical signals routed - I'm really only concerned with the via placement with respect to the signal layers I'm currently working on, not the planes to which they are connecting. In the end, when I inspect the Gerber files, I would often find large slots in the ground and power planes that were created by adjacent vias. I would then have to go back and rework these sections to try to adjust the via placement. I now periodically go back when working on a design and inspect the power and ground planes. This way, I find that the routing is not so dense and it is easier to adjust the vias to remove or minimize the slots.

There is also a trade-off when trying to remove slots – when I am trying to make a connection to ground or power, one of the main objectives is to keep the trace from the component to the via as short as possible to minimize trace inductance. Often, while keeping the length short, you inevitably end up with vias in a row that lead to a slot in the plane. Many times, as long as you keep in the back of your mind the need to avoid slots, you can come off a pad in a different direction and still keep the trace length as short as possible. If you do end up with slots you cannot avoid, it may be possible to manually stitch the spaces between the vias with copper, and still meet your design rules.

Figure No. 2 (TRACE No. 1)

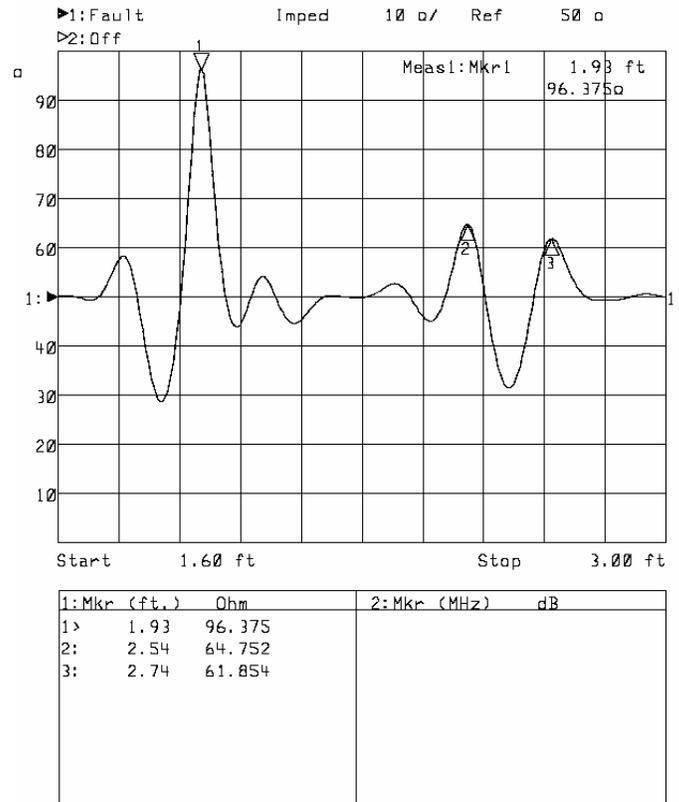


Figure No. 3 (TRACE No. 3)

