Spread Spectrum Clock (SSC) On Commercially Available Off-The-Shelf (COTS) Products & MIL-STD-461F Testing

Rhein Tech Laboratories, Inc. – February 2012
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Introduction:

A client recently inquired as to whether it would be possible to see a reduction in radiated spurious emission levels on Spread Spectrum Clock (SSC) fundamental frequency and harmonics using Peak Detectors during MIL-STD-461F testing of a COTS product, when previous FCC Part 15 testing of the COTS product proved compliance using Quasi-Peak Detectors.

Rhein Tech's Response:

If COTS with SSC products with Part 15 compliant fundamental frequencies and harmonics are tested to MIL-STD-461F using required Peak Detectors, the spectral peaks of their fundamental frequencies and harmonics should comply with MIL-STD-461F, provided the SSC timing parameters are properly configured.

A properly configured SSC would produce lower spectral peaks of the fundamental frequency and harmonics in the SSC mode than the spectral peaks of the fundamental frequency and harmonics in the non-SSC mode by levels that are dependent on the manufacturer of the SSC, modulating waveform profile, modulation rate used to modulate the fundamental frequency clock frequency in the SSC mode, spreading rate style used (down, center or up) as depicted using (Δ) in Figure 1.

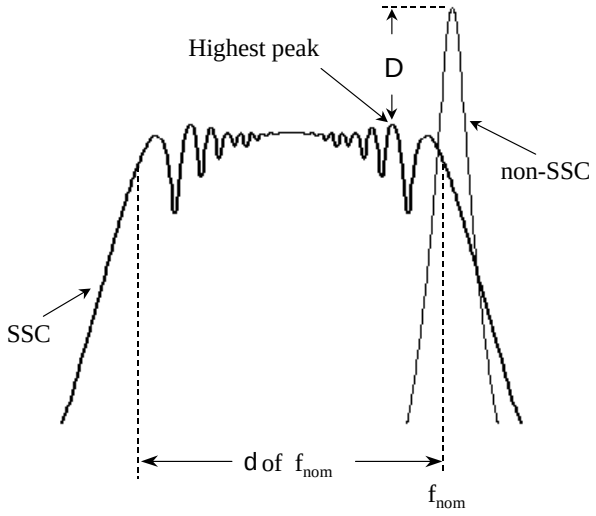

Figure 1: Spectral Fundamental Frequency Comparison [4]

Below are important SSC definitions:

1. Spreading-cycling rate (δ): The ratio of the range of spreading (dithering) frequency over the non-SSC fundamental clock frequency (f_F).

2. Modulation rate (f_M): Determines the clock-frequency spreading-cycling rate (δ).

3. Frequency spreading range (Δf): The range that the clock varies as a result of the clock-frequency spreading-cycle.

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4. Spreading style: There are three spreading styles, down-spreading, center-spreading, and up-spreading. Down-spreading is typically implemented in SSC to increase set-up and hold timing margins in digital designs that otherwise would be decreased if up-spreading and center-spreading were implemented.

   The down (δ_{DS}), center (δ_{CS}) and up (δ_{US}) spreading rates can be defined using the frequency spreading range (Δf) as follows:

   a. $Down\ spreading\ (\delta_{DS}) = \left(\frac{-\Delta f}{f_F}\right) \times 100\%$

   b. $Center\ spreading\ (\delta_{CS}) = \left(\pm\frac{1}{2\frac{\Delta f}{f_F}}\right) \times 100$

   c. $Up\ spreading\ (\delta_{US}) = \left(\frac{\Delta f}{f_F}\right) \times 100\%$

5. Modulation waveform profile: The clock frequency variation profile in time, represented by triangular waveforms, Sharkfin waveform and/or a Lexmark Waveform™ [2] (often referred to as the 'Hersey Kiss' waveform). It should be noted that sinusoidal modulation waveforms were initially used to frequency modulate SSC, however their spectral distribution peaked at both ends of the SSC's fundamental frequency and harmonics, thus reducing the amount of possible attenuation. This is as a result of the slow sinusoidal rate of change as the waveform crests towards its peaks where the spectral peaks are at their highest. Triangular waveform modulation produces good results, Sharkfin waveform modulation produces better results, and the Lexmark waveform™, with its uniform spectral peaks across the modulated waveform, produces the best amplitude reduction results for SSC.

When configuring SSC, the following timing parameters are critical for both evaluation and design [3]:

- Peak-to Peak jitter: The total percentage of spreading divided by the fundamental frequency.
- Cycle-to cycle jitter: The variation in time per cycle, dependent on the waveform profile and modulated frequency.
- Set-up and hold times: Designs that require tighter tolerances in their set and hold time margins typically use the down-spreading method, as described previously. Otherwise, care must be taken when configuring the SSC so that its configuration can support the design.

Example:

The example below will help to explain how the timing parameters of a digital design are examined.

Let us suppose that a digital design requires a 500 MHz clock configured with 2.5% total down-spread, and a 25 kHz triangular waveform profile modulation frequency. What would its peak-to-peak jitter and cycle-to-cycle jitter be?

The 500 MHz clock would have a down-spread at +/-1.25%; that is a 0.05 nanosecond peak-to-peak jitter (2 nanoseconds multiplied by 2.5%). For the cycle-to-cycle jitter, the +/-1.25% would happen during the half triangular waveform modulating frequency that is within 20 microseconds, which equates to 10,000 cycles of the 500 MHz clock. The cycle-to-cycle jitters 5000 nanoseconds, which is the peak-to-peak jitter divided by 10,000 cycles of the 500 MHz clock.

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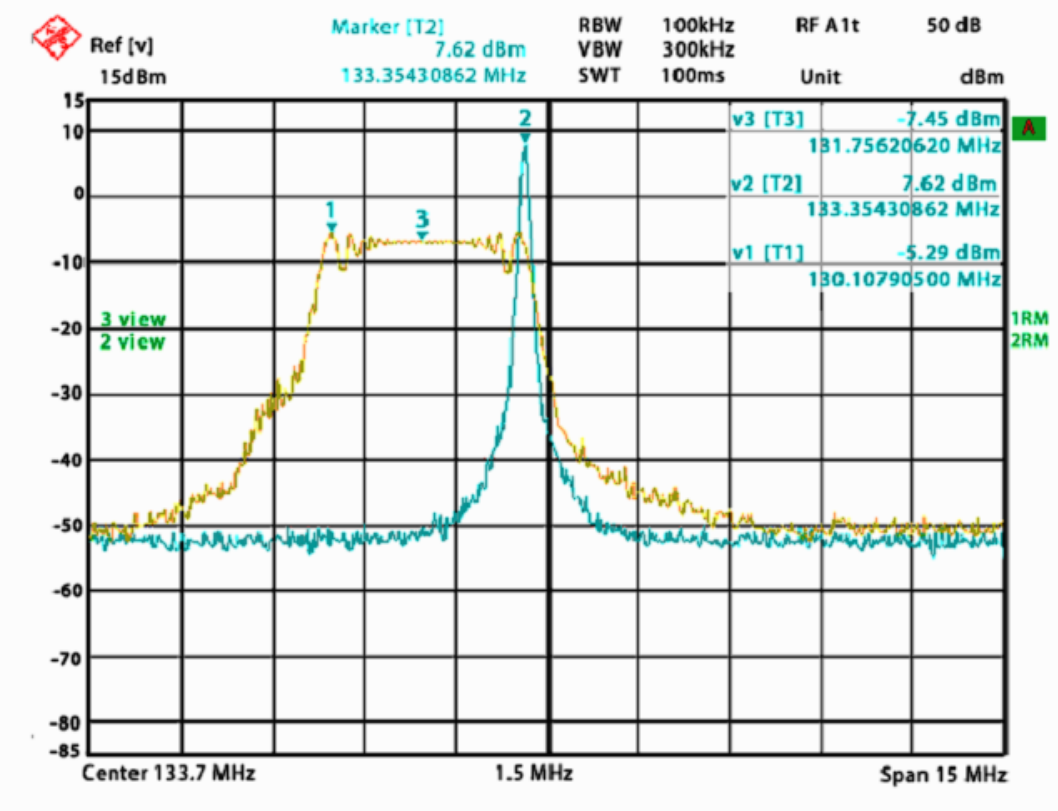

Figure 2: Clock Spectrum of the MAX9492 with and without spreading [1]

Figure 2 is an example of a Maxim clock generator operating in non-SSC mode at 133.35 MHz, and in SSC mode with a reduction in the SSC mode clock amplitude.

In conclusion, using the example above, a digital design can be evaluated in order to determine whether the SSC is properly configured to reduce the amplitude of the fundamental frequency and its harmonics when a Peak Detector is used, while at the same time ensuring that the critical set up time and hold time margins are met for a properly functioning design. It should be noted here that not all designs use SSC. Telecommunication designs generally require synchronous clocks with very strict timing specifications that SSC cannot support.

References:

1. Maxim: Application Note 3503 Clock Generation With Spread Spectrum
2. Lexmark: Lexmark Spread Spectrum Clock Generation Technology
3. Glen Dash, Ampyx LLC: Shiver Me Timers! Using Spread Spectrum Clock Generators
4. Intel® Pentium® 4 Processor CK00 Clock Synthesizer/Driver Design Guidelines.

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