Design Analysis for EMC Compliance

APPLICATION NOTE AN101

RTL Performs Design Analysis to Improve Customer's EMC Performance

Introduction

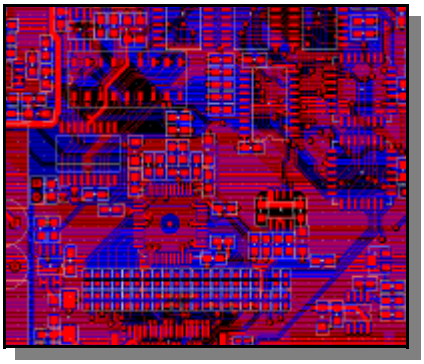
Rhein Tech Laboratories (RTL) offers various levels of design analysis for EMC compliance to your design engineers, even before your artwork is sent to be fabricated into printed circuit boards. The level of support is dependent upon your needs, but can be broadly categorized as the following:

- Schematic and layout review of existing products, providing an *EMC Modification Report* describing modifications for EMC compliance
- Consultation with customer's layout engineers during the layout process to reduce the possibility of EMC problems
- Review customer's design and provide layout and EMC testing services, giving the customer a turn-key solution guaranteeing EMC compliance to a specific standard

The following is an actual example of a design review that RTL performed for a client, with all proprietary information removed in order to protect client confidentiality. In the following case, the client desired the third option described above, that is, to have RTL perform an extensive EMC review of their design, layout the PCB and test the final product.

Description of Product

- Dimensions – 5.5" wide by 1.25" high by 6.0" long
- 10BaseT standalone network device
- Two 16 bit micro-controllers – one clocked at 10MHz, one clocked at 66MHz
- Clocks – 10, 20, 33 and 66MHz
- FPGA's
- Memory – SRAM, DRAM, FLASH
- Ethernet controllers
- Power supply requirements - +5V for most of board, +3.3V for two IC's
- Design as originally presented



contained two PCB's – one main PCB and one daughter card – multiple bus signals and clocks passing between boards

Bottom line – many clock, data and address buses with the potential for fast edge rates

Design Review – Power Distribution

The power distribution circuit of any design is one of the most critical areas as far as EMC is concerned, and is the first area looked at during the EMC analysis. Following are some of the typical questions to be asked when evaluating a design's power distribution circuit:

- Is there appropriate filtering at the power entry point to the device?
- Are there sufficient decoupling capacitors at every power pin on all IC's?
- Is there sufficient bulk capacitance periodically placed around the PCB to maintain constant DC voltage and current during times of high switching activity?
- Have the power supplies to oscillator or clock generation circuits been individually filtered?

Design Recommendations – Power Distribution

- Add a common mode filter to power supply to suppress conducted emissions through power supply cable (see Figure 1).
- Decoupling capacitors - recommend two decoupling capacitors for every power pin. Populate with values that differ by at least 100 times (for example, 0.01uF and 100pF).
- Bulk capacitors – recommend adding a minimum of ten 10uF capacitors to provide constant DC voltage and current. Distribute evenly around the PCB, but place in key high current draw locations, such as near clock synthesizers.
- Clock circuitry power supply filtering – the power supplies of all clock oscillators and clock drivers should be individually filtered as shown in Figure 2.

Design Review – PCB Stackup Notes and Recommendations

- On main PCB, two layers have no adjacent reference planes
- Power and ground planes not adjacent, high impedance - no benefit from decoupling effect of adjacent power and ground planes
- On daughter card, power and ground planes not adjacent – same problem
- Five layers have no adjacent reference plane, likely EMI radiators
- New design combines both main PCB and daughter card, eliminating radiation problems due to signals passing through connector and by creating a single low-impedance ground reference for all signals
- Power and ground planes are adjacent, creating a low-impedance/low inductance pair
- Power and ground pair simulates large decoupling capacitor, helps control common-mode EMI

Design Review—Grounding Strategy

- Implement a multipoint grounding scheme that connects the PCB ground planes to chassis ground at many locations
- Add four mounting holes to the PCB to allow four standoffs to connect the PCB to the chassis
- Place ground strips on the top and bottom layers of the board on both the left and right sides to provide additional paths to and from the PCB ground to chassis ground. Do not place solder mask at these locations. The ground strips should be connected to the PCB ground planes with numerous vias.
- The shields of all connectors should maintain a 360° connection to the front and back panels
- Insure that no paint or other insulating material is present where PCB meets enclosure, where connectors meet panels and where standoffs mount to enclosure

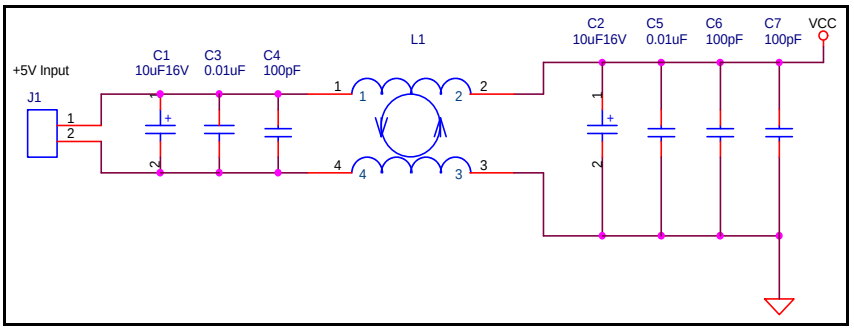


Figure 1—Recommended common mode power filter. Place immediately after power supply input connector.

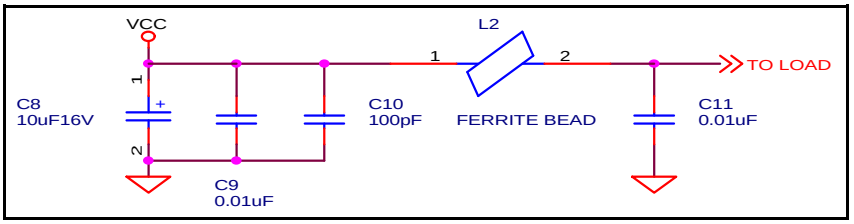


Figure 2—Recommended filter for clock oscillators and associated circuitry—add the following power supply filter to the 20MHz and 66MHz oscillators, as well as the clock driver IC

Layer 1	Top	Components/some routing
Layer 2	Inner	Routing
Layer 3	Inner	Routing
Layer 4	Inner	Routing – primarily 33MHz clocks
Layer 5	Inner	Ground
Layer 6	Inner	Routing – primarily 66MHz clocks
Layer 7	Inner	Power
Layer 8	Inner	Routing
Layer 9	Inner	Routing
Layer 10	Bottom	Components/some routing

Figure 3—Original stackup of daughter card PCB

Layer 1	Top	Components/some routing
Layer 2	Inner	Routing
Layer 3	Inner	Routing
Layer 4	Inner	Power plane
Layer 5	Inner	Routing – clocks
Layer 6	Bottom	Ground plane/ 6 passive components

Figure 4—Original stackup of main PCB

Layer 1	Top	Components/some routing
Layer 2	Inner	Ground
Layer 3	Inner	Routing
Layer 4	Inner	Routing – all clocks
Layer 5	Inner	Ground
Layer 6	Inner	Power
Layer 7	Inner	Routing – least critical signals
Layer 8	Inner	Routing
Layer 9	Inner	Ground
Layer 10	Bottom	Components/some routing

Figure 5—Recommended stackup—combines main and daughter card PCB's into single 10-layer PCB

Design Review – Network Filtering on T1 and T2 (isolation transformers w/LPF and common mode choke)

- Add capacitors to ground on all the analog differential signal lines on the transceiver side of T1 and T2. Populate with 100pF capacitors.
- Use 20 mil traces for the analog differential signal lines between T1/T2 and the transceivers. In addition, keep all other high speed signals away from the analog differential signals. Keep the traces from the RJ-45 connectors, transformers and transceivers as short as possible.
- Remove the ground plane from the area underneath the RJ-45 connectors to T1/T2. The ground plane should begin approximately from the line formed between pins 6 and 11 on T1/T2. Orient T1 and T2 such that the transformer side of these components is positioned facing the RJ-45 connectors.

Design Review – Clock and Data/ Address Bus Filtering

- 20MHz Ethernet net - Because this net fans out to four loads, a series resistor close to the source is recommended. Utilize a daisy chain configuration to connect this net to the four loads. Place an AC termination and a pull-up

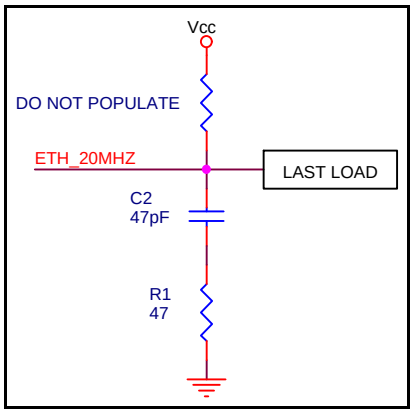


Figure 6—20MHz Ethernet net termination

resistor to Vcc at the last load (populate the AC termination as shown above, do not populate the pull-up resistor). Also, keep stub lengths short when connecting the load and try to keep all loads as close together as possible during parts placement.

Summary and General Design Recommendations

- Stackup – make sure that every routing layer has an adjacent reference plane
- Create adjacent power/ground pairs in order to benefit from the decoupling effects - also lowers impedance, reduces common mode EMI
- Eliminate daughter cards if possible. If not, place low-speed, non-critical circuitry on daughter card
- Grounding – multi-point ground scheme to chassis, 360° connections around all I/O connectors
- Filtering – consider individual localized filters for oscillators and clock driver IC's
- Decoupling – attempt to place pads for two decoupling caps on every power pin (second cap can optionally be populated if needed, value should be at least 100 times smaller than first cap)

Conclusion

Add more passive filtering components than you think is necessary. These do not have to be populated, but will prove very valuable if a device fails EMC testing and needs to be debugged in the lab. For example, add 2 or even 3 decoupling capacitors at power pins, but only populate one during the first build. Also, add series damping elements to high-speed data and clock lines. These may be populated with very small resistors or even zero ohms, but will give a lot of flexibility when it comes to debugging. In addition, all input/ output connectors should have some type of filtering – at a minimum, small capacitance to ground on every line very close to the connector pins. When the device passes EMC testing, all unused component footprints can be removed before the production order of PCB's or during a future revision.

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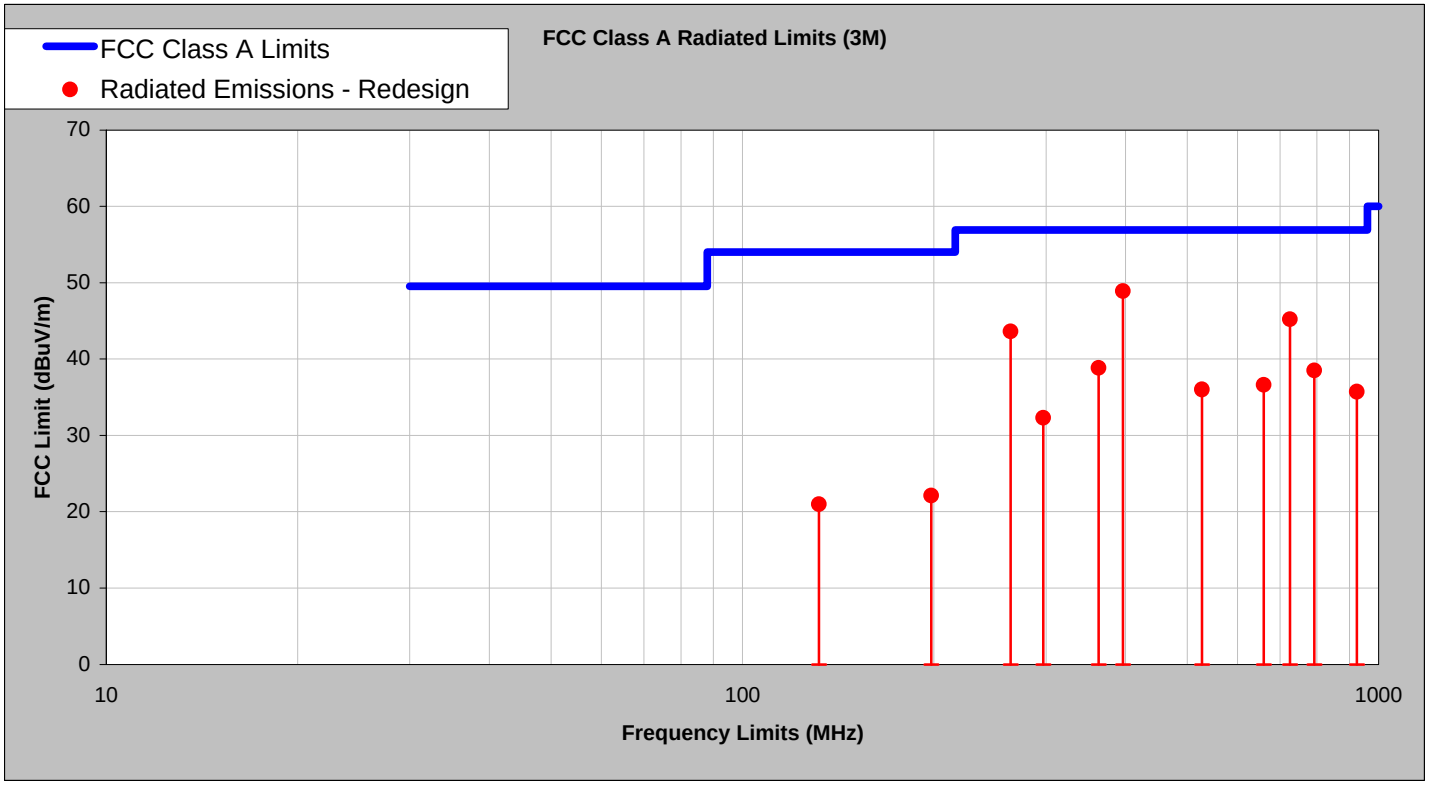

Figure 7—FCC Class A Radiated Emissions Limit and Device Data